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REMARKS

This is a preliminary amendment to be entered with a Request For Continued Examination, and represents a full and timely response to the Advisory Action mailed on July 2, 2004 and the final Office Action mailed on April 9, 2004. Through this preliminary amendment, claims 1, 4-5, 11, 14-16, 23-25, 28-30, and 35-37 have been amended, and claim 31 has been cancelled without prejudice, waiver, or disclaimer. Reconsideration and allowance of the application and pending claims are respectfully requested.

I. Objection to Drawings

In the Advisory Action, the following statement was made with regard to the drawing objections:

> Examiner has considered Applicant's remarks for the drawing objection and has not found them to be persuasive. Contrary to Applicant's remarks, it would have been clear to one skilled in the art that, due to the direction of the area, the transistor 362 of Figs. 3A and 3B is in fact shown as an N-channel and that transistor 364 is in fact shown as a P-channel. Similar, due to the direction of the arrows for the remaining transistors, such are deem to be improperly shown. Thus, the drawing objections have not been overcome.

Applicant has amended the figures to comport with enhancement mode transistor designations where the body is connected to the substrate, as disclosed in several embodiments of Applicant's application. Additionally, Applicant has enclosed Exhibits A and B for the convenience of the Examiner and to support the drawing changes that have been made. Exhibit A includes two pages from a textbook used in a course presented at a university campus on analog and digital based microelectronic circuit

design. The book is entitled, "Microelectronic Circuits, Second Edition" by Adel S. Sedra and Kenneth C. Smith. Exhibit B is a page taken from a similar university course textbook. The book is entitled, Microelectronics, Digital and Analog Circuits and Systems, by Jacob Millman. Both Exhibits A and B reveal a simplified circuit designation used to convey an enhancement mode CMOS structure (either PMOS or NMOS) where the substrate is connected to the body, as also disclosed in the Applicant's application. As shown in Exhibit A, Fig. 7-16a reveals an NMOS circuit where the substrate is represented with an arrow pointing in a direction from drain (at the top) to source (bottom). Fig. 7-16b shows a PMOS structure, where the arrow is pointing in a direction from source (top) to drain (bottom). Similarly, Fig. 8-27a of Exhibit B shows a PMOS transistor designation (Q3) where the arrow representing the substrate points in a direction from the source to the drain, and an NMOS circuit designation (Q2) where the arrow points from the drain to the source.

Relating the above to a couple of examples of transistors represented in Applicant's drawings, please refer to FIG. 3A, transistor 362. As shown, the transistor 362 takes on a configuration as shown in Exhibits A and B for PMOS transistors. In other words, the arrow representing the substrate is pointing toward the gate, from source to drain. The fact that the source is from the voltage divider side (*e.g.*, from resistor 346) is reflected in the specification on page 14, lines 1 and 2. Thus, transistor 362 is shown in one embodiment as a P-type, enhancement mode transistor where the substrate is connected to the base.

As another example, please refer to FIG. 3A and transistor 364. Transistor 364 takes on a configuration as shown in Exhibits A and B for an NMOS transistor. That is,

the arrow points away from the gate, in a direction from drain to source. Such a configuration is known to those skilled in the art as an enhancement mode NMOS transistor where the substrate is connected to the body.

Thus, in that the drawings comport with accepted practice in representing transistors, Applicant respectfully submits that the objection to the drawings has been overcome. Further, Applicant respectfully requests that the drawing objections be withdrawn.

II. Objection to Specification

The Office Action alleges the following with regard to the objection to the specification:

> The amendment to the specification has not been approved. Such still is not consistent with what would be understood by one skilled in the art or with the above discussion concerning the drawings.

Applicant submits that the specification, through this amendment, has been amended to correct inaccuracies in the drain and/or source designations. Applicant respectfully submits that through these amendments to the specification, the objection to the specification has been overcome. Thus, Applicant respectfully requests that the objection to the specification be withdrawn.

III. Claim Rejections Under 35 USC § 112

Applicant appreciates the Examiner's indication that the rejection to the claims under 35 U.S.C. § 112, first paragraph has been overcome. The Office Action notes the following with regard to the 35 U.S.C. § 112, second paragraph rejection:

> With respect to the rejection under 35 U.S.C. § 112, second paragraph, Examiner responds by stating it is not understood how this is an issue of lexicography. There are no terms at issue for which there is a specific, new or special definition provided for is the specification. Further, Applicant can be his/her own lexicographer only if the use of such is not repugnant to the known meaning. Clearly, referring to all of these elements as "output nodes" or "output signals" would be seen by one skilled in the art as repugnant to the known meaning.

Applicant has amended the claims to remove reference to "output nodes" and "output signals." Since the rejection under 35 U.S.C. § 112, second paragraph has been overcome, Applicant respectfully requests that the rejection be withdrawn.

IV. Rejection of Claims 1, 10, 11, 13-24, 28 and 29 Under 35 USC § 102 (b)

A. Statement of the Rejection

Claims 1, 10, 11, 13-24, 28 and 29 are rejected under 35 U.S.C. Section 102(b) as allegedly being anticipated by *Lee* (U.S. Pat. No. 5,889,437).

Applicant respectfully traverses this rejection.

B. Discussion of the Rejection

It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §102 as being anticipated based upon a single reference, the reference must

disclose, teach, or suggest, either implicitly or explicitly, all elements/features/steps of the claim at issue. *See, e.g., In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

Independent Claim 1

In the present case, not every feature of the claimed invention is represented in the *Lee* reference. The final Office Action alleged the following:

> Lee discloses, in Fig. 7, a circuit comprising: "a first input stage" having "a first input transistor (M41)", "a first complementary transistor (M42)", "a first discharging transistor (M45)" and "a charging transistor (M47)"; "a first control signal (UP)"; "a first reference signal (UP-upper score)"; "a second input stage" having "a second input transistor (M43)", a complementary transistor (M44)", "a second discharging transistor (M46)" and "a charging transistor (M50)"; "a second control signal (DN)"; "a second reference signal (DN—upper score)"; and "a loop filter (R1, C1, C2)", all connected and operating similarly as recited by Applicant.

Not every feature of independent claim 1 is disclosed in the *Lee* reference. In particular, *Lee* does not disclose at least the features of "***the first complementary transistor is operable to receive a first reference signal having a substantially constant voltage***," or "***the second complementary transistor operable to receive a second reference signal having a substantially constant voltage***" as recited in claim 1. The final Office Action alleged the following:

> Further, with respect to Applicant's remarks concerning the "reference signal". However, it is notoriously well known that the complement of a signal can reasonably be considered a reference for that signal. It appears Applicant is giving too much limitation to the "reference signal".

The circuit in Fig. 7 of Lee receives a switching signal as the first reference signal (UP—upper score) and the second reference signal (DN—upper score). The UP—upper score signal is not a "first reference signal having a ***substantially constant voltage***," as recited in claim 1. Likewise, the DN—upper score signal is not a "second reference signal having a ***substantially constant voltage***," as recited in claim 1. Such a circuit configuration in one embodiment disclosed in Applicant's specification and claimed enables "an output signal having reduced switching noise" to be produced. In that *Lee* fails to disclose the features emphasized above, Applicant respectfully submits that the rejection to claim 1 be withdrawn.

Because independent claim 1 is allowable over *Lee*, dependent claims 2-11, and 13-25 are allowable as a matter of law for at least the reason that the dependent claims 2-11 and 13-25 contain all the elements of their respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

In addition, Applicant also respectfully traverses the rejections of the dependent claims on other grounds. For example, in claim 15, it is apparent that *Lee* uses a **RC filter** on the output, rather than a "filter" comprised of "transistors configured to provide capacitance and resistance" as claimed. Thus, Applicant respectfully requests that the rejection to claim 15 be withdrawn.

As another example, it is apparent that *Lee* does not disclose "where the charge pump operates with a supply voltage of less than 2.5 volts," as recited in claim 20. Thus, Applicant respectfully requests that the rejection to claim 20 be withdrawn.

As another example, it is apparent that *Lee* does not disclose "where the charge pump operates with a supply voltage of less than 1.9 volts," as recited in claim 21. Thus, Applicant respectfully requests that the rejection to claim 21 be withdrawn.

Independent Claim 28

With regard to independent claim 28, Applicant respectfully submits that independent claim 28 is allowable for at least the reason that *Lee* does not disclose at least the feature of "providing ***a substantially constant reference voltage*** to first and second complementary transistors to reduce coupling noise from the first and second switching transistors," as recited in claim 28. As described above, the circuit in Fig. 7 of *Lee* receives switching signals as the reference signal (UP—upper score and DN—upper score). Neither the UP—upper score signal nor the DN—upper score signal is ***substantially constant reference voltage***," as recited in claim 28. Since *Lee* fails to disclose the features emphasized above, Applicant respectfully submits that the rejection to claim 28 be withdrawn.

Because independent claim 28 is allowable over the prior art of record, dependent claim 29 (which depends from independent claim 28) is allowable as a matter of law.

V. Rejection of Claims 30, 32 and 38 Under 35 USC § 102 (b)

A. Statement of the Rejection

Claims 30, 32 and 38 are rejected under 35 U.S.C. Section 102(b) as allegedly being anticipated by *Kawasaki* (U.S. Pat. No. 5,955,904).

Applicant respectfully traverses this rejection.

B. Discussion of the Rejection

Applicant respectfully submits that independent claim 30 is allowable for at least the reason that *Kawasaki* does not disclose at least the features of "a second transistor pair, comprising a second switching transistor and a second complementary transistor," or "a second switching transistor gate, associated with the second switching transistor, coupled to a second control signal, and a second complementary transistor gate, associated with the second complementary transistor, being coupled to the constant reference voltage such that the second complementary transistor is indirectly controlled by the second control signal," as recited in claim 30. In particular *Kawasaki* only shows a single transistor pair. Thus, for at least these reasons, Applicant respectfully requests that the rejection to independent claim 30 be withdrawn.

Furthermore, because independent claim 30 is allowable over *Kawasaki*, dependent claims 31-38 are allowable as a matter of law for at least the reason that dependent claims 31-38 contain all features/elements of independent claim 30.

VI. Cancelled Claims

As identified above, claim 31 has been cancelled from the application through this response without prejudice, waiver, or disclaimer. Applicant reserves the right to present these cancelled claims, or variants thereof, in continuing applications to be filed subsequently.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully asserts that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

THOMAS, KAYDEN,
HORSTEMEYER & RISLEY, L.L.P.

By: _____
David Rodack; Reg. No. 47,034

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Suite 1750
Atlanta, Georgia 30339
(770) 933-9500

Exhibit A. V2

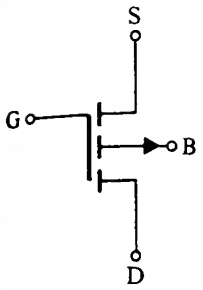


Fig. 7.15 Circuit symbol for the *p*-channel enhancement-type MOSFET.

The Role of the Substrate—The Body Effect

In many applications the substrate (or body) terminal B is connected to the source terminal, which results in the *pn* junction between the substrate and the induced channel (see Fig. 7.11) having a constant reverse bias. In such a case the substrate does not play any role in circuit operation and its existence can be ignored altogether.

In integrated circuits, however, the substrate is usually common to many MOS transistors. In order to maintain the reverse-bias condition on the substrate-to-channel junction, the substrate is usually connected to the most negative power supply in an NMOS circuit (the most positive in a PMOS circuit). The resulting reverse-bias voltage between source and body (V_{SB}) will have an effect on device operation. To appreciate this fact, observe that V_{SB} can control the channel depth in the same manner as the gate voltage in a JFET controls its channel; increasing V_{SB} depletes the channel of charge carriers. The body terminal, in effect, acts as a second gate for the MOSFET. The effect of the reverse-bias voltage V_{SB} on device operation can be described via the dependence of V_t on V_{SB}, given approximately by

$$V_t \simeq \text{constant} + \gamma\sqrt{V_{SB}} \tag{7.18}$$

where the constant part of V_t is independent of V_{SB} and γ is a device parameter that depends, among other things, on the doping of the substrate and is typically equal to 0.5 $V^{1/2}$.

Since the substrate is almost always connected to a dc supply, it will be at signal ground. Nevertheless, the source terminal may have a signal voltage on it with the result that a signal voltage appears between body and source. Now since the body acts as a second gate, such a signal voltage v_{bs} will give rise to a drain current component. This effect, known as the *body effect*, can cause considerable degradation in circuit performance, as will be shown in a later section.

Temperature Effects

Both V_t and K are temperature-sensitive. The magnitude of V_t decreases by about 2 mV for every 1°C rise in temperature. This decrease in $|V_t|$ gives rise to a corresponding increase in drain current as temperature is increased. However, because K decreases with temperature and its effect is a dominant one, the overall observed effect of a temperature increase is a *decrease* in drain current. This very interesting result is put to use in applying the MOSFET in power circuits (Chapter 10).

Exhibit A 2/2

Breakdown and Input Protection

As the voltage on the drain is increased, a value is reached at which the substrate-to-channel junction breaks down. Such a breakdown is of the avalanche type and causes the current to increase rapidly, just as in the case of the JFET (see Fig. 6.11).

In the MOSFET another kind of breakdown occurs when the gate-to-source voltage exceeds about 50 V. This is the breakdown of the gate oxide and it results in permanent damage to the device. Although 50 V is high, it must be remembered that the MOSFET has a very high input impedance, and thus small amounts of static charge accumulating on the input capacitor (between gate and source) can cause this breakdown voltage to be exceeded.

To prevent the accumulation of static charge on the input capacitor of a MOSFET, gate protection devices are usually included at the input of MOS integrated circuits (such as the input terminals of a CMOS logic gate). The protection mechanism invariably makes use of clamping diodes (see Fig. 15.44).

Simplified Circuit Symbols

When the substrate is connected to the source, the simplified circuit symbols of Fig. 7.16 will be used to represent the enhancement-type MOSFET. The difference between these circuit symbols and those for the depletion-type MOSFETs in Fig. 7.3 and 7.8b should be noted. The extra bar in the depletion-device symbol is used to signify the existing channel.

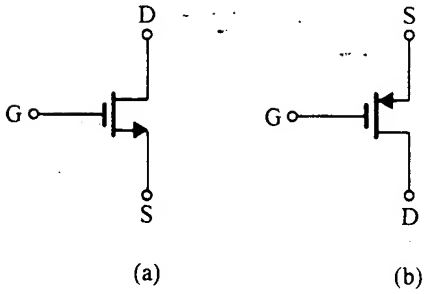


Fig. 7.16 Simplified circuit symbols for enhancement-type MOSFETs in which the body is connected to the source.

An Alternative View of the Depletion MOSFET

The depletion MOSFET studied in Section 7.1 can be considered as an enhancement device with a negative (for NMOS) threshold voltage. The negative threshold voltage, which is equal to the pinch-off voltage, is a result of the implanted channel. This view of the depletion device can be appreciated by comparing its i_D-v_{GS} characteristic in Fig. 7.7 with that of the enhancement device in Fig. 7.12. By adopting this viewpoint, the depletion-type device can be represented by the same equations presented above for the enhancement-type MOSFET with the parameter I_{DSS} given by

$$I_{DSS} = KV_t^2 \tag{7.19}$$

Recapitula

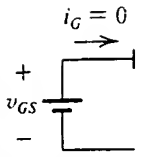


Fig. 7.17 No

Exercises

Exhibit B

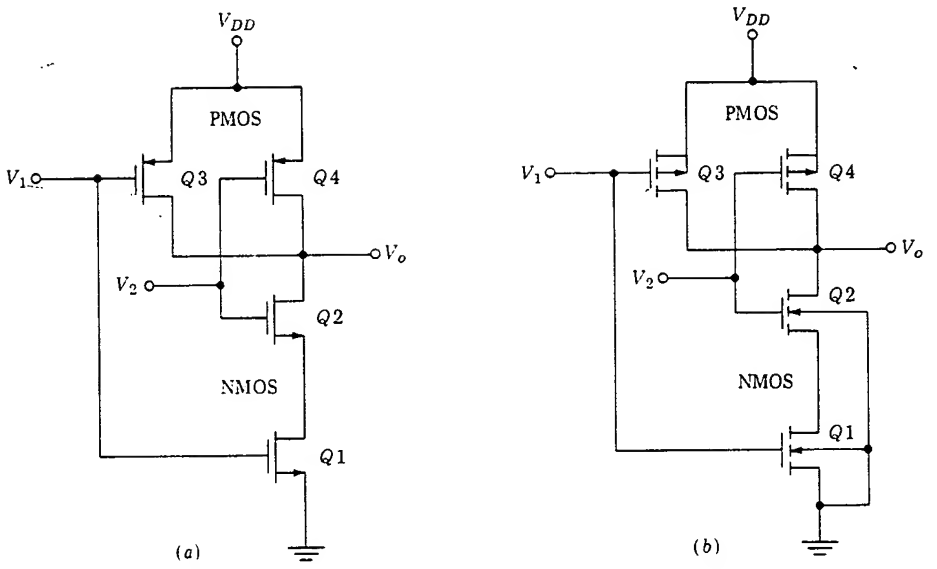


Figure 8-27 (*a*) A CMOS NAND gate. (*b*) An alternative drawing of this gate, showing the substrate connections. The *n* substrate of the PMOS is connected to the most positive supply voltage (V_{DD}) and the *p* well of the NMOS is tied to the most negative voltage (ground, for the above circuit).

CMOS Properties

The desirable features of CMOS gates are the following.

1. The quiescent (static) power dissipation is extremely small (a few nanowatts). Appreciable power is absorbed only when switching from one state to the other. At 1-MHz switching rate the dynamic power increases to a few milliwatts in a 50-pF load (about the same as in a Schottky low-power gate).
2. The noise immunity is better than 40 percent of V_{DD}. Note that, for V_{DD} = 10 V in the inverter transmission characteristic of Fig. 8-26*b*, a noise voltage of 4V superimposed upon $V(0) = 0$ reduces the output from $V(1) =$ 10 V by only a fraction of a volt.
3. Propagation delay is about 50 ns per gate, allowing 10-MHz clock rates. Hence, CMOS is faster than MOS but slower than TTL logic.
4. The fan-out is very high, in excess of 50.
5. The logic swing is V_{DD}, independent of the fan-out.
6. A single power supply is required, and it can be a simple and inexpensive system (because of the small standby current).
7. If V_{DD} = 5 V, then CMOS is TTL compatible.
8. The temperature stability is excellent (Fig. 8-26*b*).

The above advantages are offset by the increased cost because of the additional processing steps required. Also the density of gates for a given chip area is decreased since CMOS requires that PMOS and NMOS devices appear in pairs. For example,[16] a four-input NAND gate requires about 50 mil^2 for CMOS, 30 mil^2 for TTL (low power, Schottky), 11 mil^2 for PMOS, and 5.6 mil^2 for I^2L (Sec. 9-13).

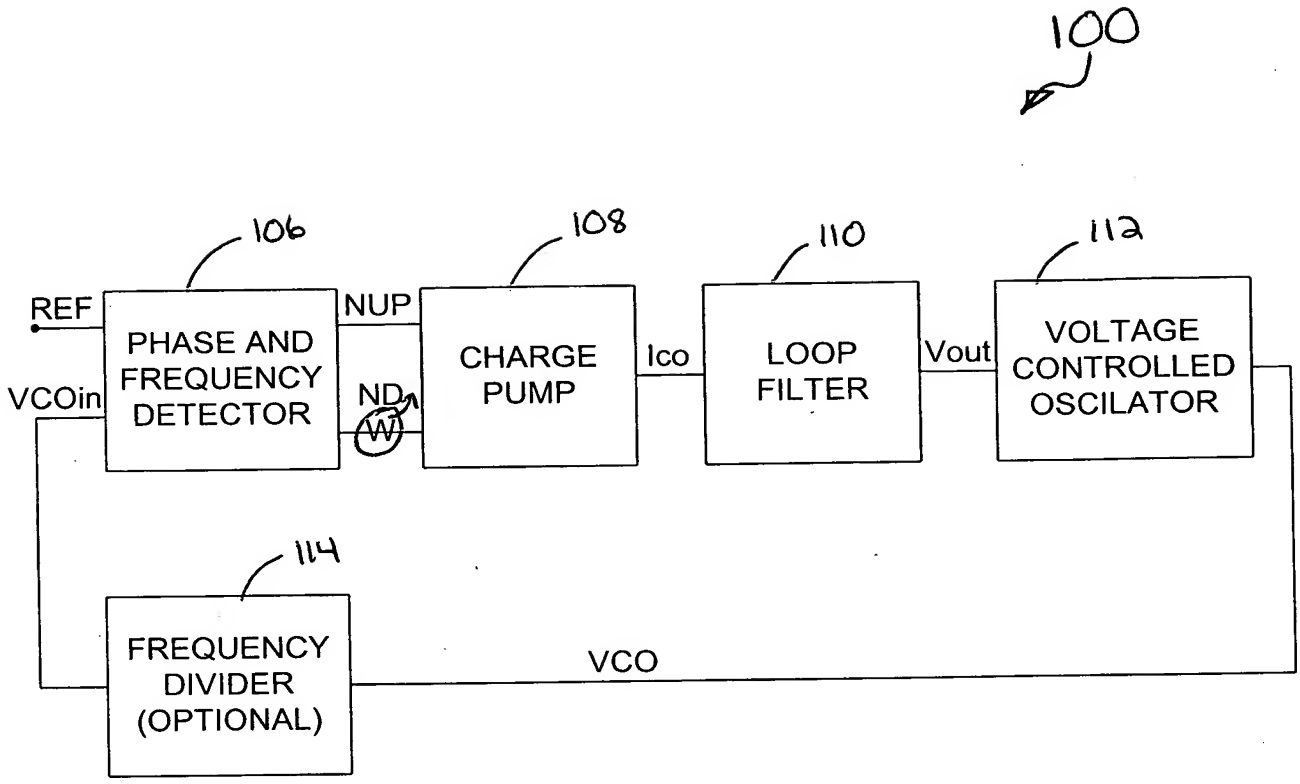
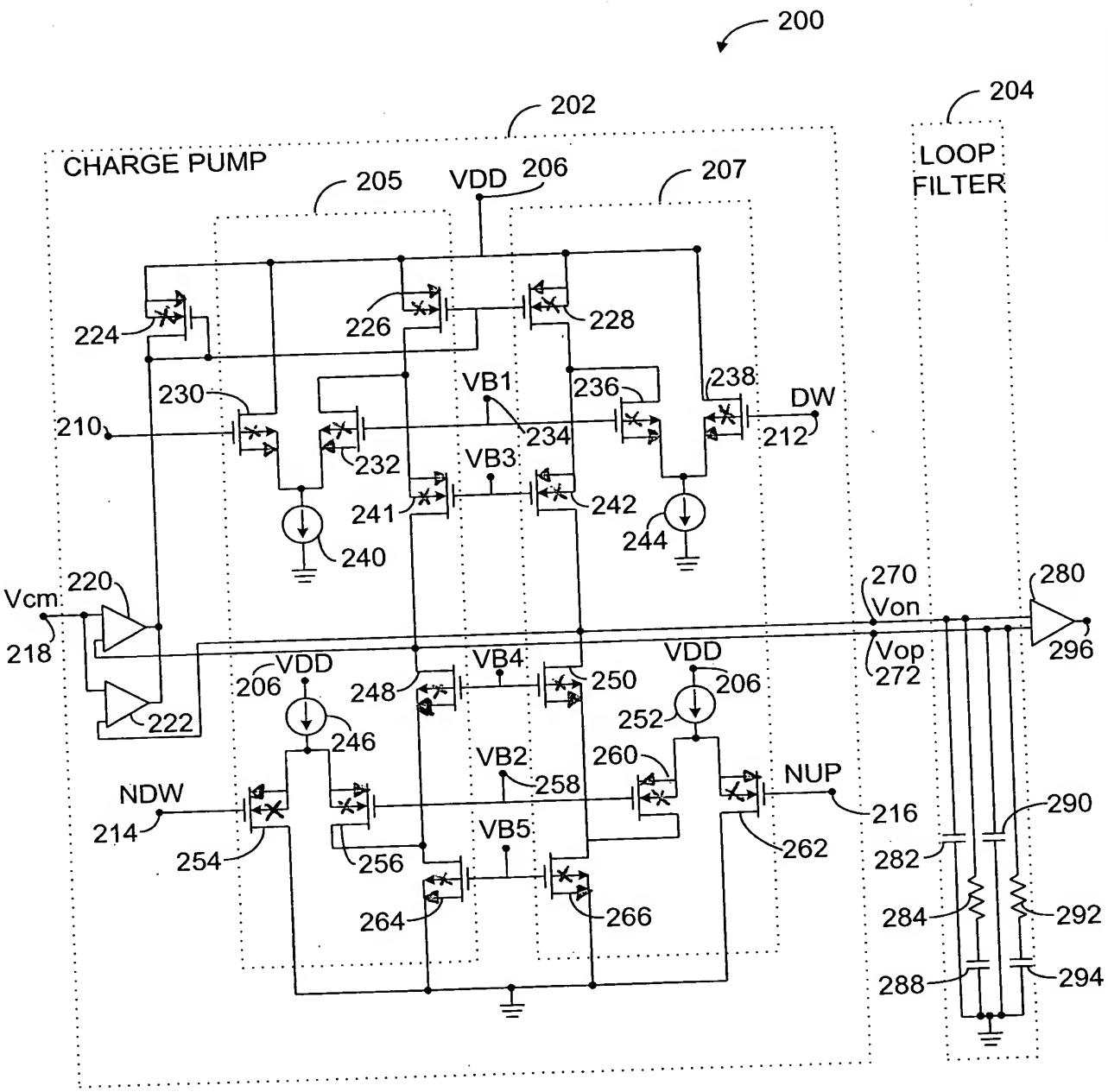


FIGURE 1


200
202
CHARGE PUMP
204
LOOP FILTER
205
VDD
206
207
224
226
228
230
VB1
236
238
DW
210
234
212
232
VB3
241
242
240
244
Vcm
220
218
222
270
Von
280
296
Vop
272
VDD
206
VB4
248
250
VDD
206
246
252
VB2
260
258
NUP
NDW
214
216
254
256
VB5
262
264
266
290
282
284
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288
294

FIGURE 2

Marked-up Drawing

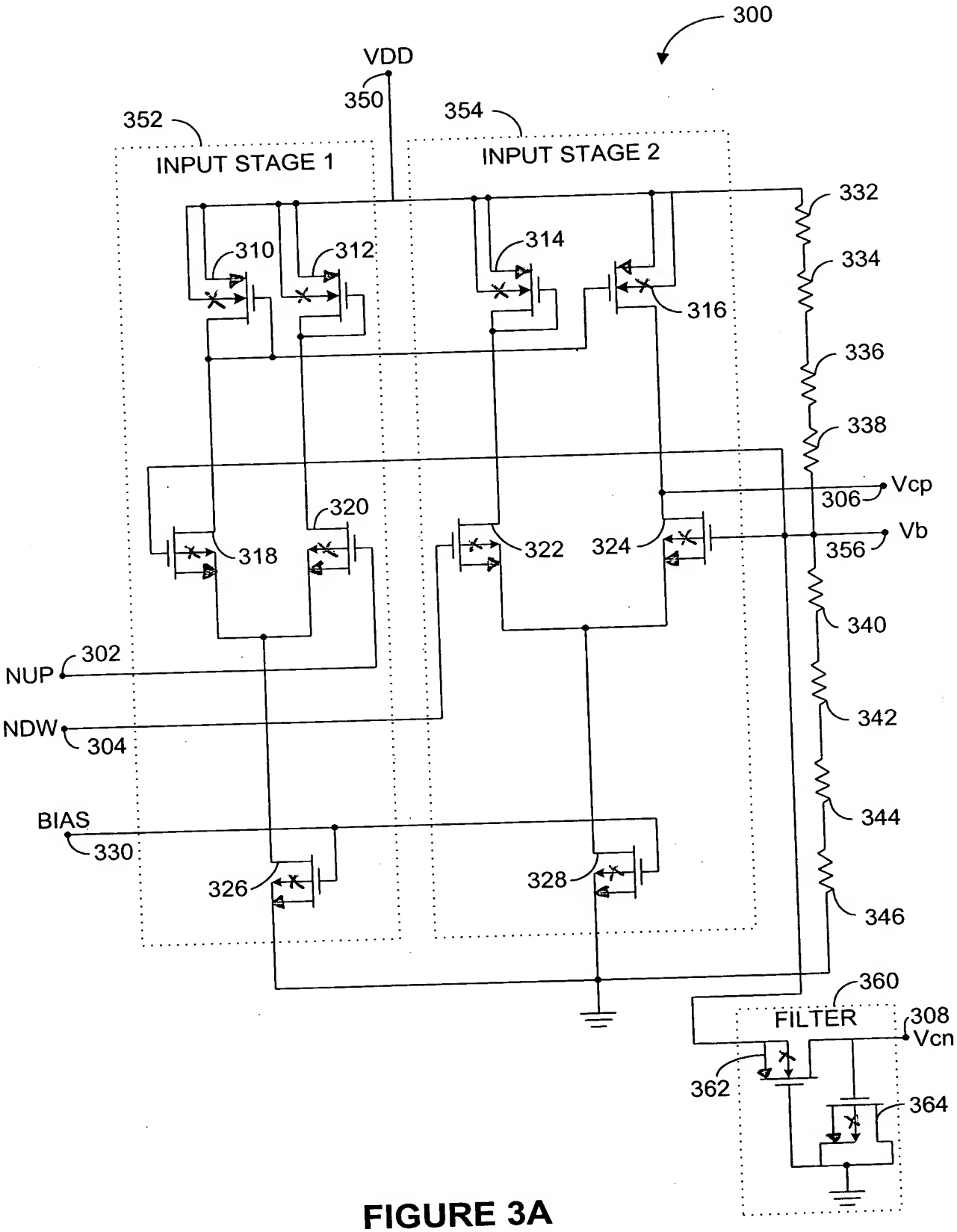


FIGURE 3A

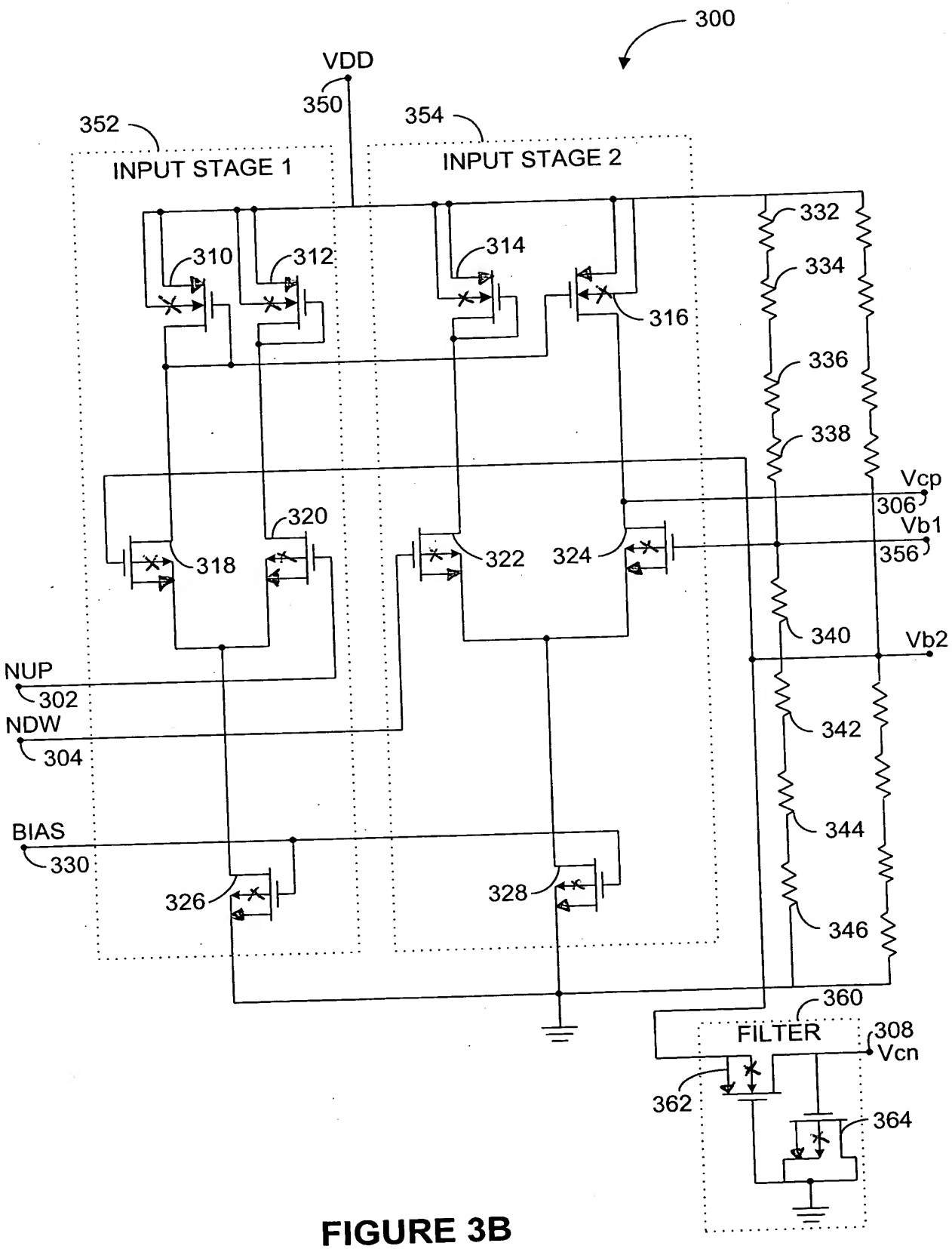
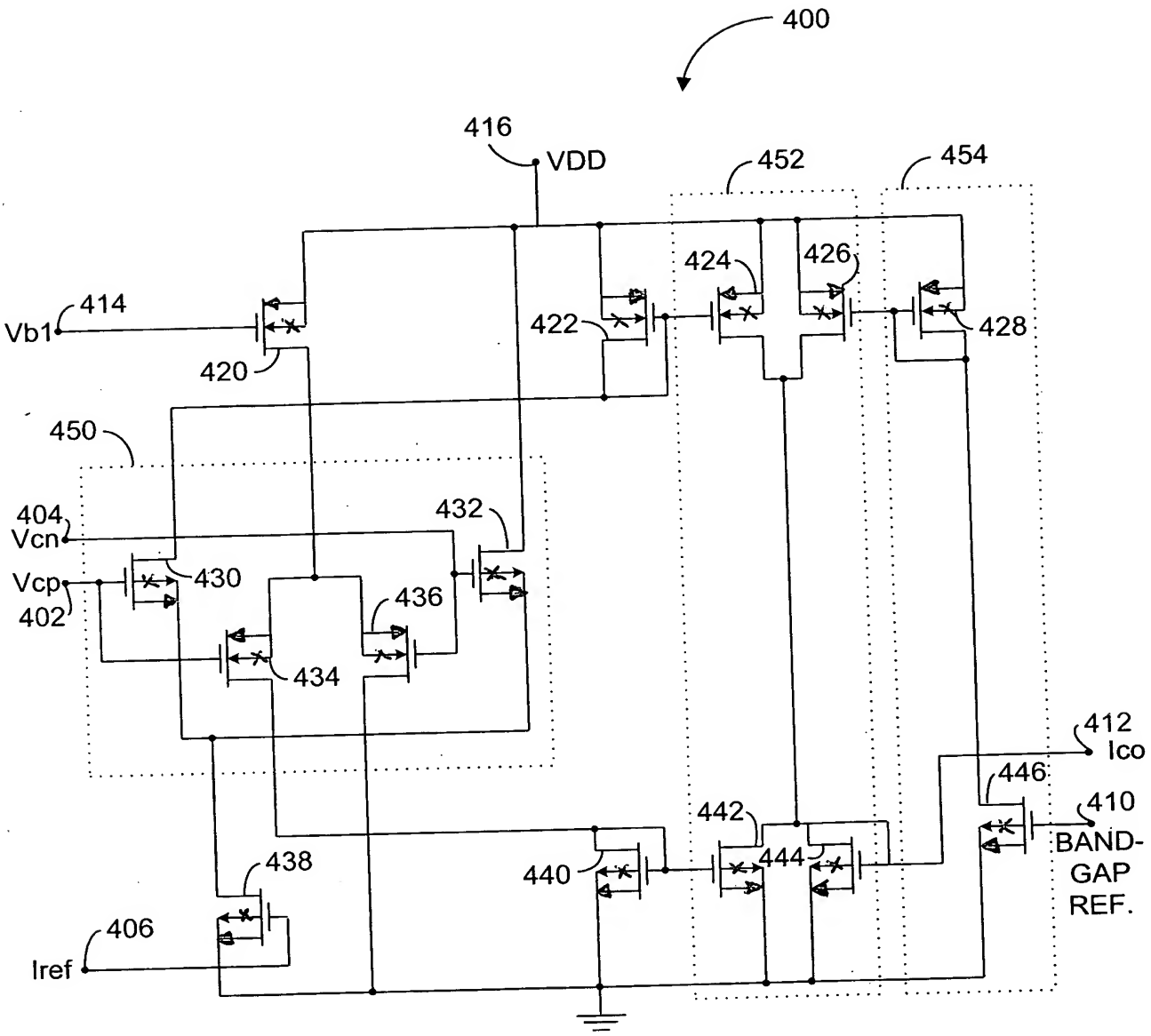

300
VDD
350
352
INPUT STAGE 1
354
INPUT STAGE 2
310
312
314
316
318
320
322
324
326
328
330
BIAS
NUP
302
NDW
304
332
334
336
338
340
342
344
346
Vcp
306
Vb1
356
Vb2
360
FILTER
308
Vcn
362
364

FIGURE 3B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424
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414
Vb1
422
428
420
450
404
Vcn
432
Vcp
402
430
436
434
412
Ico
446
442
410
BAND-
GAP
REF.
438
440
444
406
Iref

FIGURE 4

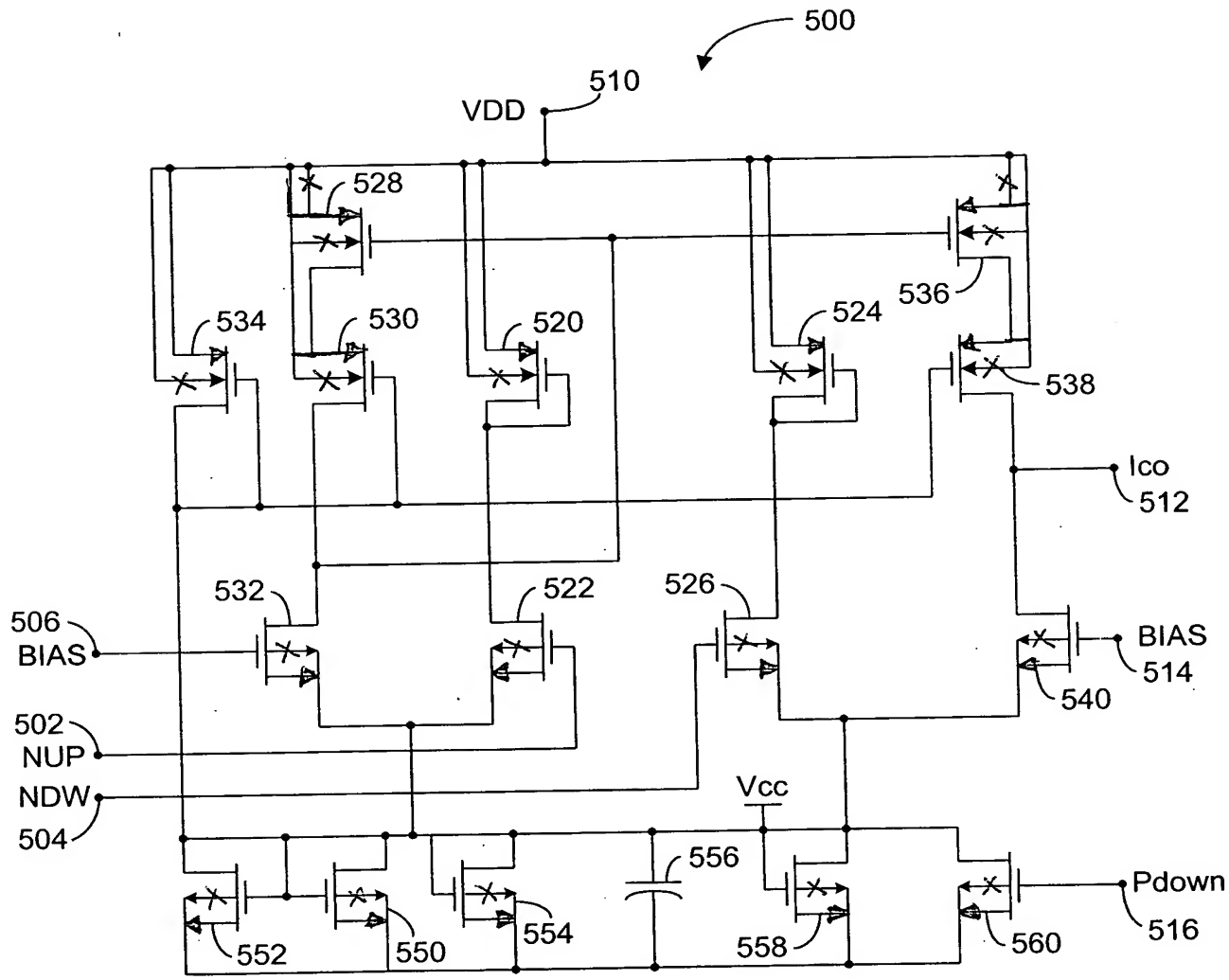
500
510
VDD
528
534
530
520
524
536
538
Ico
512
532
522
526
506
BIAS
BIAS
514
540
502
NUP
NDW
504
Vcc
556
552
550
554
558
560
Pdown
516

FIGURE 5